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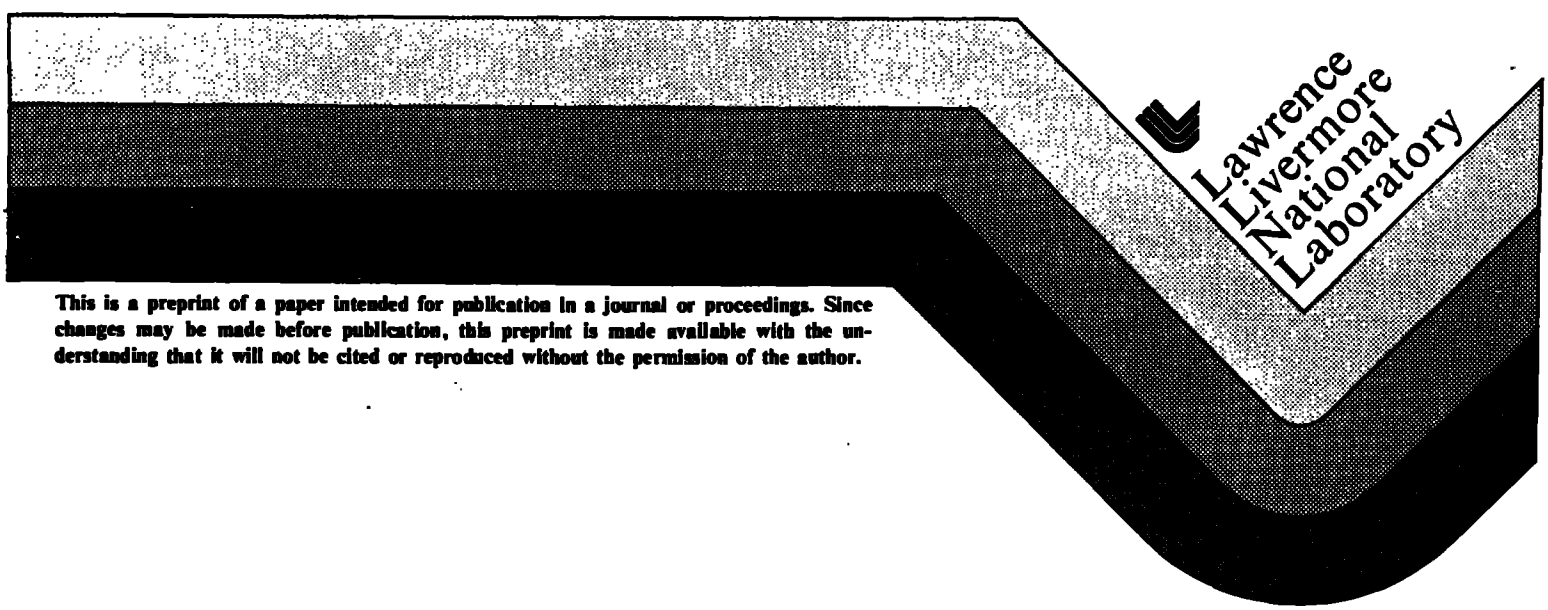

Use of Surrounding p-Type Ring to Decrease Backgate Biasing in GaAs MESFET's*

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Abstract-The sensitivity to backgate biasing of two MESFET designs, one with an implanted, surrounding p-ring and one without,were compared. A highly resistive p-like surface layer, possibly arising from the uncapped anneal, is thought to be the agent of the backgating. The addition of the surrounding p-ring results in greatly decreased backgate biasing.

I. INTRODUCTION

Backgate biasing, the partial or complete pinching off of GaAs MESFET's by a negatively biased structure elsewhere on the chip, has been widely reported. Traps in the underlying semi-insulating material [1],[3] or the presence of p-type surface layer[2],[7] have been identified as possible mechanisms for the backgate biasing. In the past, workers have sought to reduce the backgate biasing by carefully selecting their substrates [3] or modifying the intervening SI regions with trap creating ion implantation [4]. The use of a p-type region adjacent to the drain stripe and at the drain potential has also been reported to decrease the effects of backgating [5]. The uncapped annealing process which we use has consistently resulted in a highly resistive, p-like surface layer and a related high degree of backgate biasing. In this paper we report on a modified approach using a transistor structure which has been surrounded by a p-type ring that is electrically connected to the source electrode and that decreases backgate biasing sensitivity.

The motivation for examining this transistor structure arose from three characteristics noted on our circuits:1) the voltage at which backgating occurred showed little or no threshold;2) grounded n-wells between the transistor and the backgate electrode gave no significant backgating protection;and 3)whereas n-well to n-well leakage was

negligible,p-well to p-well measurements typically showed 5 megaohms/square. These observations suggested that a surface layer extending to a depth greater than the channel implant and having p-like properties was the agent of the backgating process,and that MESFET's could function well in the presence of such a layer if first, the layer's sheet resistance were high enough and second, the local electrical potential of the layer were the same as the source potential of the MESFET; i.e. a short could be established between the MESFET source and the highly resistive p-like surface layer.

II. EXPERIMENT AND RESULT

The two MESFET geometries described differ by the addition of a surrounding p-ring to the "RSP" design. Fig. 1 shows the implanted regions and the gate for the two tested designs. In the case of the RSP design the source surrounds the MESFET and the outer edge of the source adjoins a surrounding p-ring (ohmic metal, not shown in the figure, connects the source to the p-ring); the "RDN" MESFET is surrounded by its drain and is entirely n-type. One might expect that because of its positive outer electrode the RDN design would enjoy better backgating protection than a similarly all n-type construction but with the surounding electrode being a source. Even so the RDN was more subject to backgating than the RSP design. In testing each design, two types of backgating electrodes were used, one p-type and one n-type. The choice of electrode type made no difference in the observed backgating, but at strongly negative backgate voltages, current flowed from the n-type electrode to the RSP MESFET. Fig. 2 shows the locations of the two backgating contacts; this particular pair was chosen because it offered equidistant p and n type contacts. Two intervening n-wells, used for close spaced backgate tests, were present; they were allowed to float and do not alter the salient features of the results.

The essential features of the sample preparation are as follows:

1)Implantation of n+ source and drain areas into (100) LEC GaAs.

2)Implantation of 1.2×10^{12} at 60keV plus 5.3×10^{12} at 200keV of $^{30}Si^{+}$ to form the channel implant.

3)Successive implantations of $3x10^{13}$ each at 40keV and 100keV $^{9}Be^{+}$ to form the p-rings on the RSP samples.

4)Proximity annealing for 30 minutes at 850C in a loosely covered boat containing InAs as a source of arsenic pressure.

5)Evaporation of AuGe/Ni/Au and alloying of ohmic contacts. In the RSP case the source contact was extended to also contact the p-ring.

6)Gate recess etching followed by evaporation of Cr/Au gates.

7)A polyimide dielectric layer and second-level metal complete the fabrication process.

The shift in the V_{gs}=0 drain characteristic for the MESFET having no p-ring protection (RDN) is shown in Fig.3(a). With as little as -10V applied to the p-type backgate, the drain current drops 20% and severe looping appears. With a backgate voltage of -30V, the drain current drops 40%; the small size of the further decline as the drain voltage is reduced to -39.2V(the limit of the power supply) shows the onset of backgating saturation. When the backgate voltage was applied to the n-type backgate, the results were identical. Neither the p-type nor the n-type backgate contacts showed any current (the minimum observable current was 10 microampere).

Identical measurements on the p-ring protected MESFET (RSP) showed a dramatic improvement; see Fig. 3(b). For -30V applied to the p-type backgate electrode, the reduction in drain current was less the 3%. Between -30V and -39.2V, the drain current begins to drop, although the shift is much less than in the RDN case. Again the backgate current is less than the minimum observable value. An interesting difference in behavior is present in the n-type backgate case. The behavior is essentially identical for backgate voltages down to -33.2V where current from the n-backgate to the RSP source began to flow. The current increased to 1ma at -36.2V where the measurement was stopped to avoid possibly damaging the MESFET.

III. CONCLUSIONS

The three characteristics mentioned in the introduction suggested the presence of a p-like surface layer and this is consistent with the backgating protection demonstrated by the RSP design. The surrounding p-ring ties the local potential of the p-like layer beneath the channel to that of the MESFET's source electrode. Such local pinning of the potential would allow the fabrication of noninteracting MESFET's on a GaAs substrate if the ensuing p-ring to p-ring currents were not excessive. An attractive aspect of the p-ring structure is that it is expected to effectively decrease backgating despite variations in substrate material and processing.

The nature of the p-like layer is not elucidated by these measurements, and we have avoided labeling it as a p-layer. We have observed that proton implantation caused a sharp decrease in the p-well to p-well leakage, and this indicates that a surface effect is involved with a possible additional but probably smaller bulk contribution. The out diffusion of EL2 traps reported in annealed samples could result in a p-layer extending more than a micrometer into the wafer [6].

The currents that flow between negative n-wells and positive p-ring MESFET's have a nonlinear dependence on bias and contact spacing. We have made measurements (for the large spacing that is available on this chip) showing that the addition of a p-ring surrounding the n-well will suppress this current. This indicates that current flow problems between p-ring MESFET's will not be severe, and will allow the use of such devices in improved high-voltage, linear IC's.

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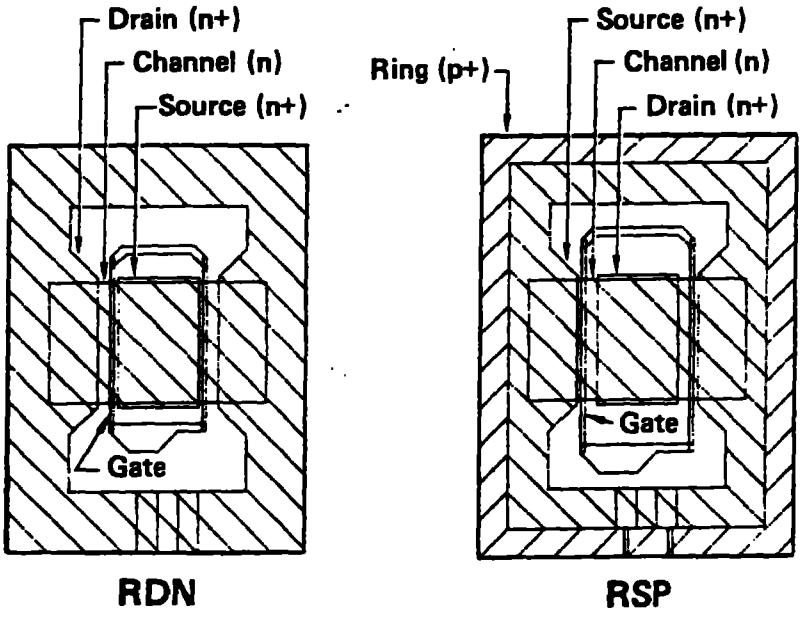


Fig. 1. Geometries of the implanted regions and the gates for the two tested MESFET's. The RDN pattern consists of an outer n+ drain ring and an inner n+ source rectangle joined by a lightly implanted rectangular channel. The functions of the n+ regions of the RSP pattern are reversed and an outer p-type ring is added.

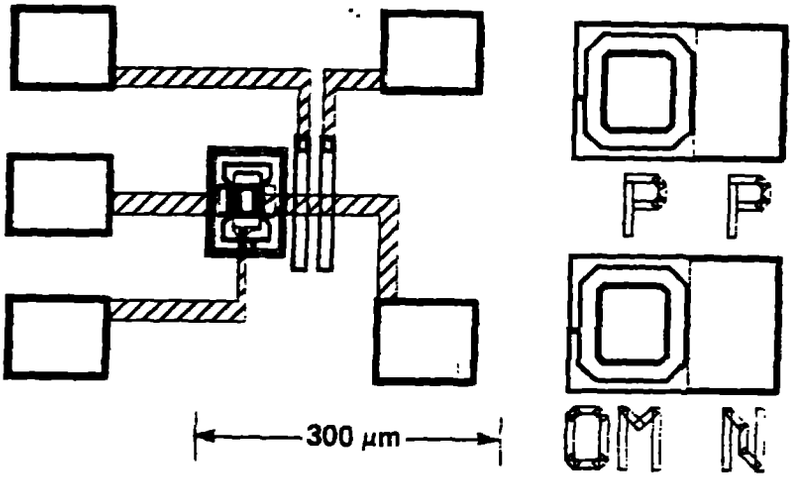
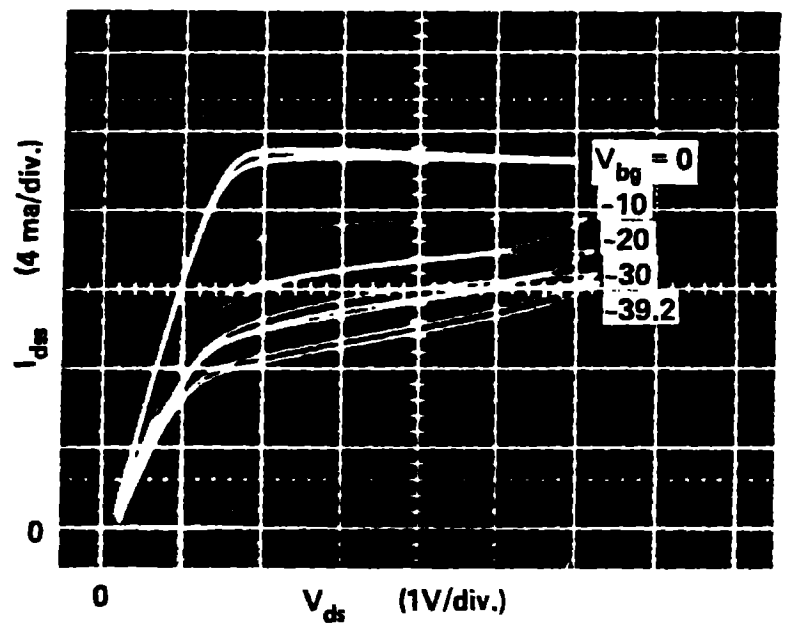
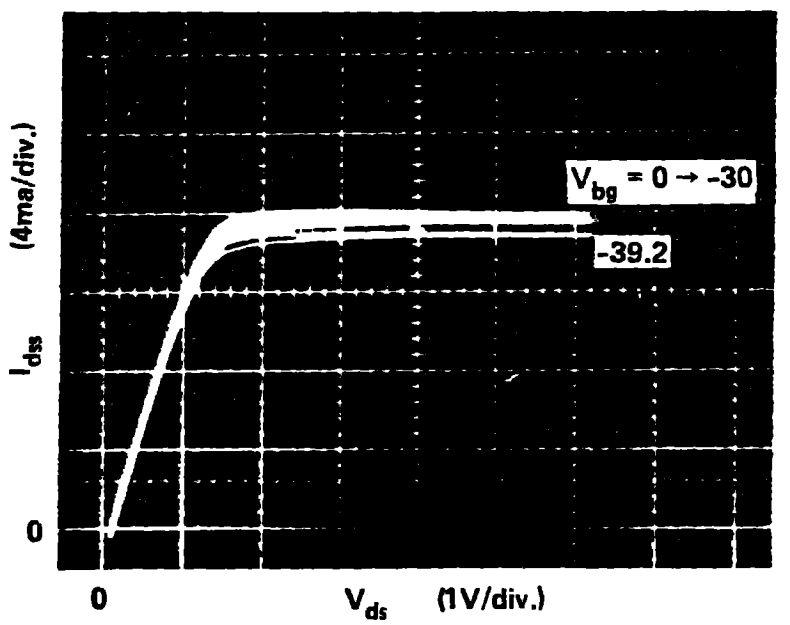


Fig. 2. The MESFET, at the left, was backgate biased by either the p-region (P-P) or the n-region (OM-N) at the right. The crosshatched areas are second level metal. The two n+ stripes just right of the MESFET were used for near-pattern backgating tests;in this case they were left floating.



(a)



(b)

Fig. 3. The V_{gs}=0 drain current characteristic is shown for values of backgate voltage of 0V, -10V, -20V, -30V, and -39.2V applied to the p-type backgate. The RDN design, which has no protective p-ring, shows both severe backgating and looping(a). The RSP design, with its surrounding p-ring, shows greatly reduced backgating and no increased looping (b).